## FEATURES

Meets EIA RS-485 Standard
30 Mbps Data Rate
Single 5 V Supply
-7 V to +12 V Bus Common-Mode Range
High Speed, Low Power BiCMOS
Thermal Shutdown Protection
Short-Circuit Protection
Driver Propagation Delay: 10 ns
Receiver Propagation Delay: 15 ns
High-Z Outputs with Power Off
Superior Upgrade for LTC1485

## APPLICATIONS

Low Power RS-485 Systems
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

## GENERAL DESCRIPTION

The ADM1485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both RS-485 and RS-422 EIA Standards. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are three-stated.
The ADM1485 operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.
Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM1485 driver features high output impedance when disabled and also when powered down.

REV. F
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## FUNCTIONAL BLOCK DIAGRAM

8-Lead


This minimizes the loading effect when the transceiver is not being used. The high impedance driver output is maintained over the entire common-mode voltage range from -7 V to +12 V .
The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).
The ADM1485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.
The ADM1485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at typical data rates of 30 Mbps while low skew minimizes EMI interference.
The part is fully specified over the commercial and industrial temperature range and is available in PDIP, SOIC, and small MSOP packages.

## ADM1485—SDEGFFGATIONS $\left(V_{C C}=5 \mathrm{~V} \pm 5 \%\right.$. All specifications $\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$, unless otherwise noted. $)$

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRIVER |  |  |  |  |  |
| Differential Output Voltage, $\mathrm{V}_{\mathrm{OD}}$ |  |  | 5.0 | V | $\mathrm{R}=\infty$, Test Circuit 1 |
|  | 2.0 |  | 5.0 | V | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{R}=50 \Omega$ (RS-422), Test Circuit 1 |
|  | 1.5 |  | 5.0 | V | $\mathrm{R}=27 \Omega$ (RS-485), Test Circuit 1 |
| $\mathrm{V}_{\text {OD3 }}$ | 1.5 |  | 5.0 | V | $\mathrm{V}_{\text {TST }}=-7 \mathrm{~V}$ to +12 V , Test Circuit 2 |
| $\Delta\left\|\mathrm{V}_{\mathrm{OD}}\right\|$ for Complementary Output States |  |  | 0.2 | V | $\mathrm{R}=27 \Omega$ or $50 \Omega$, Test Circuit 1 |
| Common-Mode Output Voltage $\mathrm{V}_{\text {OC }}$ |  |  | 3 | V | $\mathrm{R}=27 \Omega$ or $50 \Omega$, Test Circuit 1 |
| $\Delta\left\|\mathrm{V}_{\mathrm{OD}}\right\|$ for Complementary Output States |  |  | 0.2 | V | $\mathrm{R}=27 \Omega$ or $50 \Omega$ |
| Output Short-Circuit Current ( $\mathrm{V}_{\text {OUT }}=$ High $)$ | 35 |  | 250 | mA | $-7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq+12 \mathrm{~V}$ |
| Output Short-Circuit Current ( $\mathrm{V}_{\text {OUT }}=$ Low $)$ | 35 |  | 250 | mA | $-7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{O}} \leq+12 \mathrm{~V}$ |
| CMOS Input Logic Threshold Low, V ${ }_{\text {INL }}$ |  |  | 0.8 | V |  |
| CMOS Input Logic Threshold High, $\mathrm{V}_{\text {INH }}$ | 2.0 |  | $\pm 1.0$ | V |  |
| Logic Input Current (DE, DI) |  |  |  | $\mu \mathrm{A}$ |  |
| RECEIVER |  |  |  |  |  |
| Differential Input Threshold Voltage, $\mathrm{V}_{\text {TH }}$ | -0.2 |  | +0.2 | V | $-7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq+12 \mathrm{~V}$ |
| Input Voltage Hysteresis, $\Delta \mathrm{V}_{\mathrm{TH}}$ |  | 70 |  | mV | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ |
| Input Resistance | 12 |  |  | $\mathrm{k} \Omega$ | $-7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq+12 \mathrm{~V}$ |
| Input Current (A, B) |  |  | 1 | mA | $\mathrm{V}_{\text {IN }}=+12 \mathrm{~V}$ |
|  |  |  | -0.8 | mA | $\mathrm{V}_{\mathrm{IN}}=-7 \mathrm{~V}$ |
| CMOS Input Logic Threshold Low, $\mathrm{V}_{\text {INL }}$ |  |  | 0.8 | V |  |
| CMOS Input Logic Threshold High, $\mathrm{V}_{\text {INH }}$ | 2.0 |  |  | V |  |
| Logic Enable Input Current ( $\overline{\mathrm{RE}})$ |  |  | $\pm 1$ | $\mu \mathrm{A}$ |  |
| CMOS Output Voltage Low, $\mathrm{V}_{\text {OL }}$ |  |  | 0.4 | V | $\mathrm{I}_{\text {OUT }}=+4.0 \mathrm{~mA}$ |
| CMOS Output Voltage High, $\mathrm{V}_{\mathrm{OH}}$ | 4.0 |  |  | V | $\mathrm{I}_{\text {OUT }}=-4.0 \mathrm{~mA}$ |
| Short-Circuit Output Current | 7 |  | 85 | mA | $\mathrm{V}_{\text {OUT }}=\mathrm{GND}$ or $\mathrm{V}_{\text {CC }}$ |
| Three-State Output Leakage Current |  |  | $\pm 1.0$ | $\mu \mathrm{A}$ | $0.4 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 2.4 \mathrm{~V}$ |
| POWER SUPPLY CURRENT |  |  |  |  |  |
| $\mathrm{I}_{\mathrm{CC}}$ (Outputs Enabled) |  | 1.0 | 2.2 | mA | Digital Inputs $=$ GND or $\mathrm{V}_{\text {CC }}$ |
| $\mathrm{I}_{\mathrm{CC}}$ (Outputs Disabled) |  | 0.6 | 1 | mA | Digital Inputs $=$ GND or $\mathrm{V}_{\mathrm{CC}}$ |

Specifications subject to change without notice.

## TIMING SPECIFICATIONS $\left(V_{C C}=5 \mathrm{~V} \pm 5 \%\right.$. All specifications $\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAx }}$, unless otherwise noted. $)$

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRIVER <br> Propagation Delay Input to Output $\mathrm{t}_{\text {PLH }}, \mathrm{t}_{\text {PHL }}$ Driver $\mathrm{O} / \mathrm{P}$ to $\overline{\mathrm{O} / \mathrm{P}} \mathrm{t}_{\text {SKEW }}$ Driver Rise/Fall Time $t_{R}, t_{F}$ Driver Enable to Output Valid Driver Disable Timing Matched Enable Switching $\left\|\mathrm{t}_{\mathrm{AZH}}-\mathrm{t}_{\mathrm{BZL}}\right\|,\left\|\mathrm{t}_{\mathrm{BZH}}-\mathrm{t}_{\mathrm{AZL}}\right\|$ Matched Disable Switching $\left\|\mathrm{t}_{\mathrm{AHZ}}-\mathrm{t}_{\mathrm{BLZ}}\right\|,\left\|\mathrm{t}_{\mathrm{BHZ}}-\mathrm{t}_{\mathrm{ALZ}}\right\|$ | 2 | $\begin{aligned} & 10 \\ & 1 \\ & 8 \\ & 10 \\ & 10 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 5 \\ & 15 \\ & 25 \\ & 25 \\ & 2 \\ & 2 \end{aligned}$ | ns <br> ns <br> ns <br> ns <br> ns <br> ns <br> ns | $\mathrm{R}_{\text {LDIFF }}=54 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=100 \mathrm{pF}$, Test Circuit 3 <br> $\mathrm{R}_{\mathrm{LDIFF}}=54 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=100 \mathrm{pF}$, Test Circuit 3 <br> $\mathrm{R}_{\text {LDIFF }}=54 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=100 \mathrm{pF}$, Test Circuit 3 <br> $\mathrm{R}_{\mathrm{L}}=110 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Test Circuit 4 <br> $\mathrm{R}_{\mathrm{L}}=110 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Test Circuit 4 <br> $\mathrm{R}_{\mathrm{L}}=110 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Test Circuit 4* <br> $\mathrm{R}_{\mathrm{L}}=110 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Test Circuit 4* |
| RECEIVER <br> Propagation Delay Input to Output $\mathrm{t}_{\text {PLH }}, \mathrm{t}_{\text {PHL }}$ <br> Skew $\left\|t_{\text {PLH }}-\mathrm{t}_{\text {pHL }}\right\|$ <br> Receiver Enable $\mathrm{t}_{\mathrm{EN} 1}$ <br> Receiver Disable $\mathrm{t}_{\mathrm{EN} 2}$ <br> Tx Pulse Width Distortion <br> Rx Pulse Width Distortion |  | 15 <br> 5 <br> 5 <br> 1 <br> 1 | $\begin{aligned} & 30 \\ & 5 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \text { Test Circuit } 5 \\ & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \text { Test Circuit } 5 \\ & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, \text { Test Circuit } 6 \\ & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega \text {, Test Circuit } 6 \end{aligned}$ |

[^0]
## ABSOLUTE MAXIMUM RATINGS*

| ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) |  |
| :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | -0.3 V to +7 V |
| Inputs |  |
| Driver Input (DI) | .-0.3 V to $\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}$ |
| Control Inputs ( $\mathrm{DE}, \overline{\mathrm{RE}}$ ) | -0.3 V to $\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}$ |
| Receiver Inputs (A, B) | -9 V to +14 V |
| Outputs |  |
| Driver Outputs (A, B) | -9 V to +14 V |
| Receiver Output | -0.5 V to $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$ |
| Power Dissipation 8-Lead MSOP | 900 mW |
| $\theta_{\mathrm{JA}}$, Thermal Impedance | $206^{\circ} \mathrm{C} / \mathrm{W}$ |
| Power Dissipation 8-Lead PDIP | 500 mW |
| $\theta_{\mathrm{JA}}$, Thermal Impedance | $130^{\circ} \mathrm{C} / \mathrm{W}$ |
| Power Dissipation 8-Lead SOIC | 450 mW |
| $\theta_{\mathrm{JA}}$, Thermal Impedance | $170^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range |  |
| Commercial (J Version) | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| Industrial (A Version) | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 sec ) | $300^{\circ} \mathrm{C}$ |
| Vapor Phase (60 sec) | $215^{\circ} \mathrm{C}$ |
| Infrared (15 sec) | $.220^{\circ} \mathrm{C}$ |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table I. Transmitting

| Inputs |  | Outputs |  |
| :--- | :--- | :--- | :--- |
| DE | DI | B | A |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 0 | X | Z | Z |

Table II. Receiving

| $\overline{\mathbf{R E}}$ | Inputs <br> A-B | Outputs <br> $\mathbf{R O}$ |
| :--- | :--- | :--- |
| 0 | $\geq+0.2 \mathrm{~V}$ | 1 |
| 0 | $\leq-0.2 \mathrm{~V}$ | 0 |
| 0 | Inputs Open | 1 |
| 1 | X | Z |

## PIN FUNCTION DESCRIPTIONS

| Pin <br> No. | Mnemonic | Function |
| :--- | :--- | :--- |
| 1 | RO | Receiver Output. When enabled if A > B <br> by 200 mV , then RO = High. If A < B by <br> 200 mV, then RO = Low. <br> Receiver Output Enable. A low level <br> enables the receiver output, RO. A high <br> level places it in a high impedance state. <br> Driver Output Enable. A high level enables <br> the driver differential outputs, A and B. A low <br> level places it in a high impedance state. <br> Driver Input. When the driver is enabled, <br> a logic low on DI forces A low and B high <br> while a logic high on DI forces A high and |
| 3 | DE | DIB low. <br> Ground Connection, 0 V. |
| 5 | GND | Goninverting Receiver Input A/Driver <br> 6 |
| 7 | B | Output A. <br> Inverting Receiver Input B/Driver Output B <br> Power Supply, 5 V $\pm 5 \%$. |
| 8 | VCC |  |

## PIN CONFIGURATION



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## Test Circuits



Test Circuit 1. Driver Voltage Measurement


Test Circuit 2. Driver Voltage Measurement


Test Circuit 3. Driver Propagation Delay

## Switching Characteristics



Figure 1. Driver Propagation Delay, Rise/Fall Timing


Figure 2. Driver Enable/Disable Timing


Test Circuit 4. Driver Enable/Disable


Test Circuit 5. Receiver Propagation Delay


Test Circuit 6. Receiver Enable/Disable


Figure 3. Receiver Propagation Delay


Figure 4. Receiver Enable/Disable Timing


TPC 1. Output Current vs. Receiver Output Low Voltage


TPC 2. Output Current vs. Receiver Output High Voltage


TPC 3. Receiver Output High Voltage vs. Temperature


TPC 4. Receiver Output Low Voltage vs. Temperature


TPC 5. Output Current vs. Driver Differential Output Voltage


TPC 6. Driver Differential Output Voltage vs. Temperature, $R_{L}=26.8 \Omega$

## ADM1485



TPC 7. Output Current vs. Driver Output Low Voltage


TPC 8. Output Current vs. Driver Output High Voltage


TPC 9. Supply Current vs. Temperature


TPC 10. Rx Skew vs. Temperature


TPC 11. Tx Skew vs. Temperature


TPC 12. Tx Pulse Width Distortion


TPC 13. Unloaded Driver Differential Outputs


TPC 14. Loaded Driver Differential Outputs


TPC 15. Driver/Receiver Propagation Delays Low to High

## ADM1485

## APPLICATION INFORMATION

## Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) that specify the electrical characteristics of transceivers used in differential data transmission.
The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft . A single driver can drive a transmission line with up to 10 receivers.

In order to cater to true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of the RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended com-mon-mode range of -7 V to +12 V is defined. The most significant difference between the RS-422 and the RS-485 is the fact that the drivers may be disabled, thereby allowing more than one ( 32 in fact) to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Table III. Comparison of RS-422 and RS-485 Interface Standards

| Specification | RS-422 | RS-485 |
| :--- | :--- | :--- |
| Transmission Type | Differential | Differential |
| Maximum Cable Length | 4000 ft. | 4000 ft. |
| Minimum Driver Output Voltage | $\pm 2 \mathrm{~V}$ | $\pm 1.5 \mathrm{~V}$ |
| Driver Load Impedance | $100 \Omega$ | $54 \Omega$ |
| Receiver Input Resistance | $4 \mathrm{k} \Omega \mathrm{min}$ | $12 \mathrm{k} \Omega \mathrm{min}$ |
| Receiver Input Sensitivity | $\pm 200 \mathrm{mV}$ | $\pm 200 \mathrm{mV}$ |
| Receiver Input Voltage Range | -7 V to +7 V | $-7 \mathrm{~V} \mathrm{to}+12 \mathrm{~V}$ |
| No. of Drivers/Receivers per Line | $1 / 10$ | $32 / 32$ |

## Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.
The ADM1485 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 5. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.


Figure 5. Typical RS-485 Network

## Thermal Shutdown

The ADM1485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of $150^{\circ} \mathrm{C}$ is reached. As the device cools, the drivers are re-enabled at $140^{\circ} \mathrm{C}$.

## Propagation Delay

The ADM1485 features very low propagation delay, ensuring maximum baud rate operation. The driver is well balanced, ensuring distortion free transmission.
Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

## Receiver Open-Circuit Fail-Safe

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 6. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body ( $R-8$ )
Dimensions shown in millimeters and (inches)


Figure 7. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters

## ADM1485



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. REFERENCEONLY AND ARE NOT APPROPRIATE LOR USE LN DESIGN.

Figure 8. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body ( $\mathrm{N}-8$ )
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

| Model ${ }^{1}$ | Temperature Range | Package Description | Package Option | Brand |
| :---: | :---: | :---: | :---: | :---: |
| ADM1485JNZ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead PDIP | N-8 |  |
| ADM1485JRZ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead SOIC_N | R-8 |  |
| ADM1485JR-REEL | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead SOIC_N | R-8 |  |
| ADM1485JRZ-REEL | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead SOIC_N | R-8 |  |
| ADM1485ANZ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead PDIP | N-8 |  |
| ADM1485ARMZ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead MSOP | RM-8 | M42 |
| ADM1485ARMZ-REEL | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead MSOP | RM-8 | M42 |
| ADM1485ARMZ-REEL7 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead MSOP | RM-8 | M42 |
| ADM1485ARZ |  | 8-Lead SOIC_N | R-8 |  |
| ADM1485ARZ-REEL |  | 8-Lead SOIC_N | R-8 |  |
| ADM1485ARZ-REEL7 |  | 8-Lead SOIC_N | R-8 |  |
| ADM1485JCHIPS |  |  | Die |  |

[^1]
## REVISION HISTORY

8/12-Rev. E to Rev. F
Changed Data Rates of Up to 5 Mbps to Typical Data Ratesof 30 Mbps 1
Updated Outline Dimensions .....  .9
Changes to Ordering Guide ..... 10
9/03-Data Sheet changed from REV. D to REV. E.
Change to SPECIFICATIONS .....  2
Changes to ORDERING GUIDE .....  3
Updated OUTLINE DIMENSIONS .....  9
7/03-Data Sheet changed from REV. C to REV. D.
Changes to SPECIFICATIONS .....  2
Changes to ABSOLUTE MAXIMUM RATINGS .....  3
Updated ORDERING GUIDE .....  3
1/03—Data Sheet changed from REV. B to REV. C.
Change to SPECIFICATIONS .....  2
Change to ORDERING GUIDE .....  3
12/02-Data Sheet changed from REV. A to REV. B.
Deleted Q-8 Package. ..... Universal
Edits to FEATURES .....  1
Edits to GENERAL DESCRIPTION .....  1
Edits, additions to SPECIFICATIONS .....  2
Edits, additions to ABSOLUTE MAXIMUM RATINGS. .....  3
Additions to ORDERING GUIDE .....  3
TPCs updated and reformatted .....  5
Addition of 8-Lead MSOP Package .....  9
Update to OUTLINE DIMENSIONS .....  9


[^0]:    *Guaranteed by characterization.
    Specifications subject to change without notice.

[^1]:    ${ }^{1} Z=$ RoHS Compliant Part.

